DATA SHEET

TDA1576
FM/IF amplifier/demodulator circuit

Product specification
Supersedes data of March 1985
File under Integrated Circuits, IC01

1998 Nov 18

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FEATURES

- Symmetrical limiting IF amplifier
- Symmetrical quadrature demodulator
- Internal muting circuit
- Symmetrical AFC output
- Field strength indication output
- Detune detector
- Reference voltage output
- Electronic smoothing of the supply voltage
- Standby on/off switching circuit.

GENERAL DESCRIPTION

The TDA1576 is a monolithic integrated FM/IF amplifier circuit for use in mono and stereo FM-receivers of car radios or home sets.

QUICK REFERENCE DATA

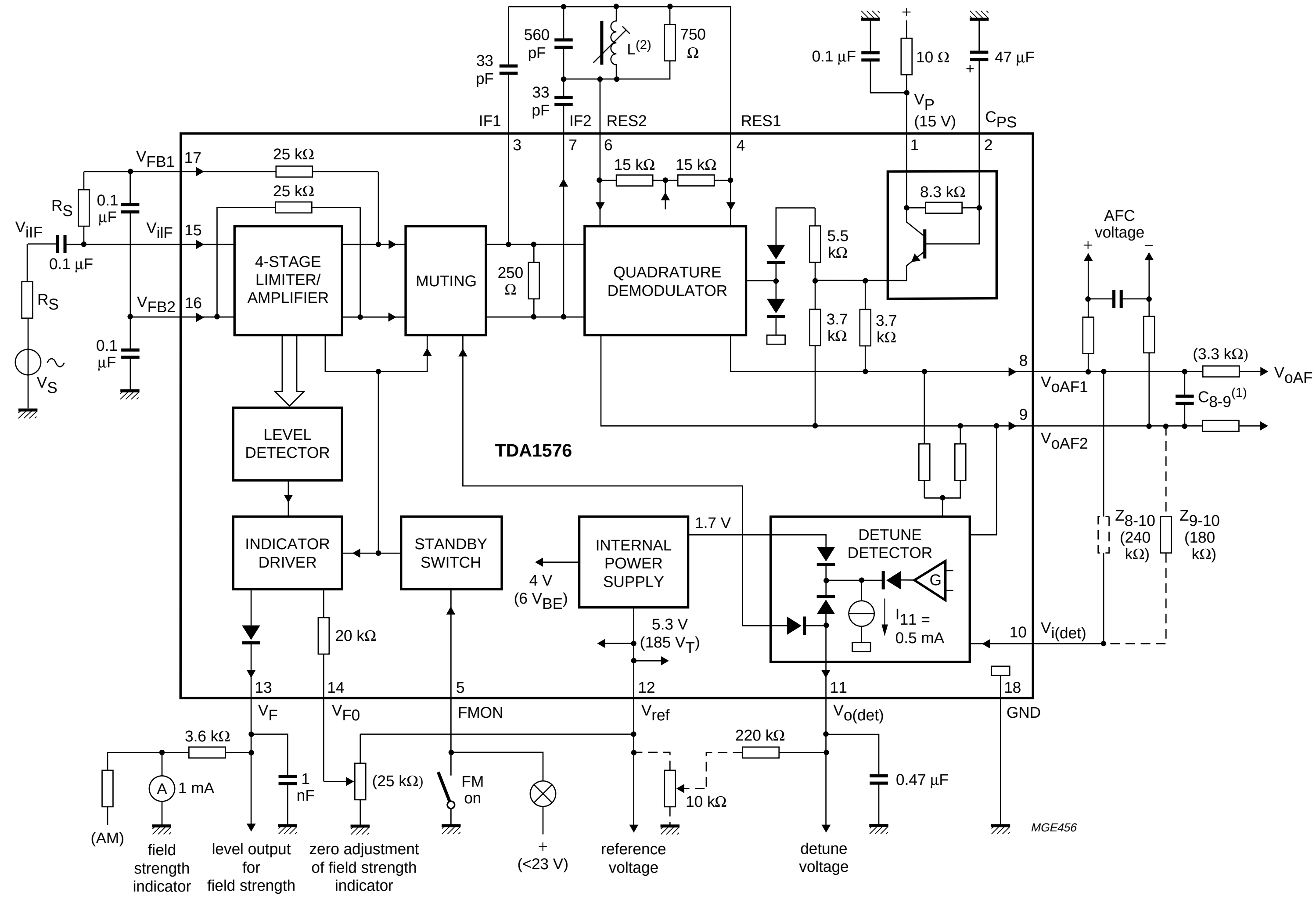
f_o = 10.7 MHz; Δf = ±22.5 kHz; f_m = 400 Hz; Q_L = 20; 50 µs de-emphasis.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_P	supply voltage (pin 1)		7.5	–	20	V
I_P	supply current	V_P = 8.5 V	–	16	–	mA
		V_P = 15 V	–	18	–	mA
$V_{iIF(rms)}$	input sensitivity (RMS value)	–3 dB before limiting	–	22	–	µV
		$\frac{S+N}{N}$ = 26 dB	–	8	–	µV
		$\frac{S+N}{N}$ = 46 dB	–	35	–	µV
$V_{oAF(rms)}$	AF output voltage (RMS value)	V_P = 8.5 V	–	67	–	mV
		V_P = 15 V	–	135	–	mV
THD	total harmonic distortion					
	single tuned circuit		–	0.1	–	%
	two tuned circuits		–	0.02	–	%
$\frac{S+N}{N}$	signal plus noise-to-noise ratio	V_{iIF} > 1 mV (RMS); V_P = 8.5 V	–	76	–	dB
		V_{iIF} > 1 mV (RMS); V_P = 15 V	–	80	–	dB
α_{AM}	AM suppression		–	50	–	dB
Δf_i	AFC offset drift		–	±3	±6	kHz
ΔV_i	field strength indication		–	90	–	dB
I_L	permissible indicator load current		–	–	2	mA
T_{amb}	operating ambient temperature		–30	–	+80	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
TDA1576	DIP18	plastic dual in-line package; 18 leads (300 mil)	SOT102-1

BLOCK DIAGRAM



(1) For 50 µs de-emphasis: C_{8-9} = 6.8 nF; for stereo operation C_{8-9} = 56 pF.

(2) L = 0.38 µH; Q_o = 70; Q_L = 20; adjusted to minimum 2nd harmonic distortion (d_2); at V_i = 1 mV; coil: 6 turns CuL (0.25 mm) on coil former KAN (C).

Fig.1 Block diagram and test circuit.

PINNING

SYMBOL	PIN	DESCRIPTION
V_P	1	positive supply voltage
C_{PS}	2	smoothing capacitor of power supply
IF1	3	IF signal to resonant circuit
RES1	4	resonant circuit input 1
FMON	5	FM-ON, standby switch
RES2	6	resonant circuit input 2
IF2	7	IF signal to resonant circuit
V_{oAF1}	8	AF output voltage 1 (0° phase)
V_{oAF2}	9	AF output voltage 2 (180° phase)
$V_{i(det)}$	10	detune detector input voltage for external audio reference
$V_{o(det)}$	11	detune detector output voltage
V_{ref}	12	reference voltage output
V_F	13	level output for field strength
V_{F0}	14	zero adjust voltage for field strength
V_{iIF}	15	FM/IF input signal voltage
V_{FB2}	16	DC feedback 2
V_{FB1}	17	DC feedback 1
GND	18	ground (0 V)

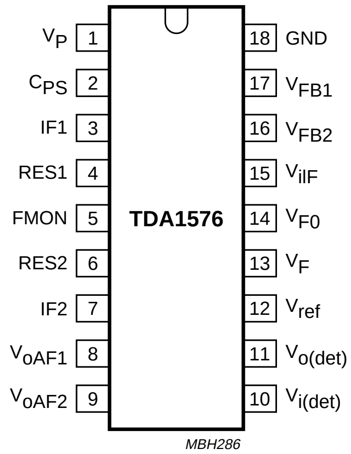


Fig.2 Pin configuration.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_P	supply voltage (pin 1)	0	23	V
V_2	voltage on pin 2	0	V_P	V
$V_{5, 14}$	voltage on pins 5 and 14	0	23	V
V_{12}	voltage on pin 12	0	7	V
V_{13}	voltage on pin 13	0	6	V
P_{tot}	total power dissipation	0	800	mW
T_{stg}	storage temperature	–55	+150	°C
T_{amb}	operating ambient temperature	–30	+80	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}a}$	thermal resistance from junction to ambient in free air	80	K/W

CHARACTERISTICS

V_P = 7.5 to 20 V; f_{IF} = 10.7 MHz; R_S = 60 Ω; f_m = 400 Hz with Δf = ±22.5 kHz; 50 μs de-emphasis (C_{8-9} = 6.8 nF); T_{amb} = 25 °C and measurements taken in Fig.1; unless otherwise specified. The demodulator circuit is adjusted at minimum second harmonic distortion for V_{iIF} = 1 mV and a deviation Δf = ±75 kHz.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
I_P	supply current without load	$I_{12} = I_{13} = 0$; V_P = 8.5 V	10	16	23	mA
		$I_{12} = I_{13} = 0$; V_P = 15 V	12	18	25	mA
IF amplifier/detector						
$V_{iIF(rms)}$	input sensitivity (RMS value; pin 15)	–3 dB before limiting	–	22	30	μV
		$\frac{S+N}{N}$ = 26 dB	–	8	–	μV
		$\frac{S+N}{N}$ = 46 dB	–	35	–	μV
$V_{oIF(p-p)}$	output voltage at pins 3 and 7 (peak-to-peak value)	$Z_{3,7}$ = 10 pF parallel to 1 MΩ	–	680	–	mV
R_{3-7}	output resistance		–	250	–	Ω
Z_{4-6}	input impedance		–	30	–	kΩ
C_{4-6}	input capacitance		–	1	–	pF
$R_{8,9}$	output resistance		–	3.7	–	kΩ
$V_{8,9}$	DC output voltage	V_P = 8.5 V	–	5.5	–	V
		V_P = 15 V	–	9.8	–	V
$V_{oAF(rms)}$	AF output voltage (RMS value)	Q_L = 20; V_P = 8.5 V	60	67	75	mV
		Q_L = 20; V_P = 15 V	120	135	150	mV
THD	total harmonic distortion					
	single tuned circuit	Q_L = 20	–	0.1	–	%
	two tuned circuits		–	0.02	–	%
$\frac{S+N}{N}$	signal plus noise-to-noise ratio (pins 8 and 9)	B = 250 Hz to 15 kHz; V_i > 1 mV (RMS); V_P = 8.5 V	–	76	–	dB
		B = 250 Hz to 15 kHz; V_i > 1 mV (RMS); V_P = 15 V	–	80	–	dB
α_{AM}	AM suppression	V_{iIF} = 10 mV; FM: 70 Hz; Δf = ±22.5 kHz; AM: 1 kHz; m = 30%; note 1	–	54	–	dB
V_{iIF}	IF input voltage	α > 40 dB	0.5	–	500	mV
α_{100}	hum suppression at f = 100 Hz	V_P = 100 mV (RMS); C_2 = 47 μF	43	48	–	dB
$\frac{\Delta V_{8-9}}{\Delta f_o}$	AFC tuning slope at Q_L = 20	V_P = 8.5 V	–	8.5	–	mV/kHz
		V_P = 15 V	–	17	–	mV/kHz

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
ΔV_{8-9}	AFC offset voltages at Q_L = 20	V_i = 1 mV; V_P = 8.5 V	–	–	±100	mV
		V_i = 1 mV; V_P = 15 V	–	–	±200	mV
		V_i = 30 µV to 500 mV (V_{ref} = 1 mV and muting); V_P = 8.5 V	–	±25	±50	mV
		V_i = 30 µV to 500 mV (V_{ref} = 1 mV and muting); V_P = 15 V	–	±50	±100	mV
Field strength output; see Fig.7						
V_i	indicator sensitivity	I_{14} = 0	0.02	–	600	mV
V_{13}	output voltage	R_{13} = 3.6 kΩ; I_{14} = 0				
		V_{iIF} = 0	–	0	200	mV
		V_{iIF} = 250 mV (RMS)	3.2	3.6	4.1	V
I_{13}	available output current		–2	–	–	mA
V_{13}	reverse voltage at output for FM off	V_5 > 3.5 V	5	–	–	V
Detuning detector						
I_{10}	quiescent input current	V_{10-9} = 0	–	20	100	nA
V_{11}	output voltage		1.8	–	5.0	V
I_{11}	maximum output current		0.35	0.5	0.65	mA
G_v	voltage gain	$\Delta V_{11}/\Delta(\pm V_{10-9})$ at I_{11} = 0.25 mA; V_P = 15 V	–	3.3	–	
V_{10-9}	input offset voltage (pin 10)	V_{11} = 2.5 V	–	20	–	mV
Reference voltage						
V_{ref}	reference voltage (pin 12)	I_{12} = –1 mA; V_P = 8.5 V	–	5.1	–	V
		I_{12} = –1 mA; V_P = 15 V	–	5.3	–	V
I_{12}	available output current		–	–2.5	–	mA
Standby switch						
V_5	input voltage for FM on		–	–	2	V
	input voltage for FM off		3.5	–	–	V
I_5	input current for FM on		–	–	–100	µA

Note

1. Simultaneously measured.

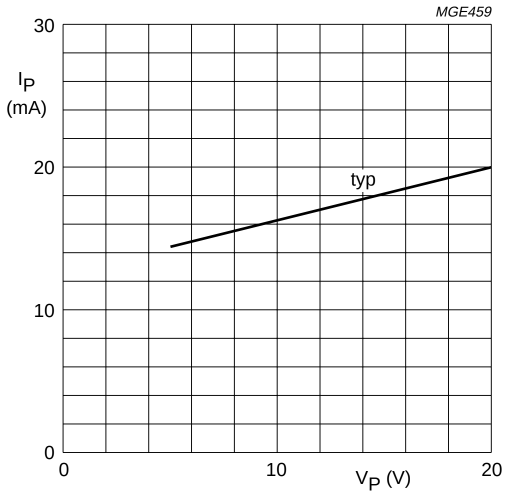


Fig.3 Supply current consumption as a function of V_P without load.

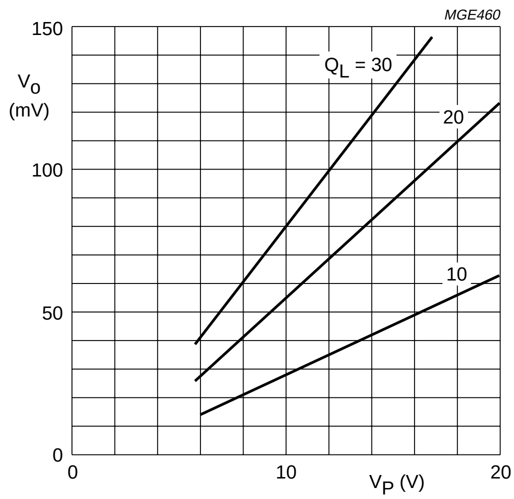


Fig.4 AF output voltage as a function of V_P; V_{iIF} = 1 mV; Δf = ±15 kHz; f_m = 400 Hz; typical values.

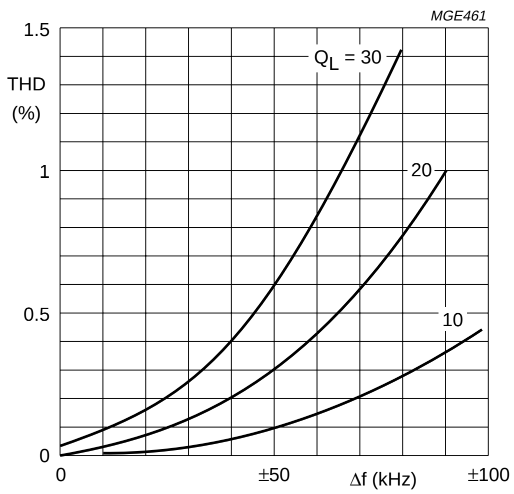


Fig.5 Total harmonic distortion for single tuned circuit; V_{iIF} = 1 mV; f_m = 400 Hz; adjusted at minimum 2^{nd} distortion; typical values.

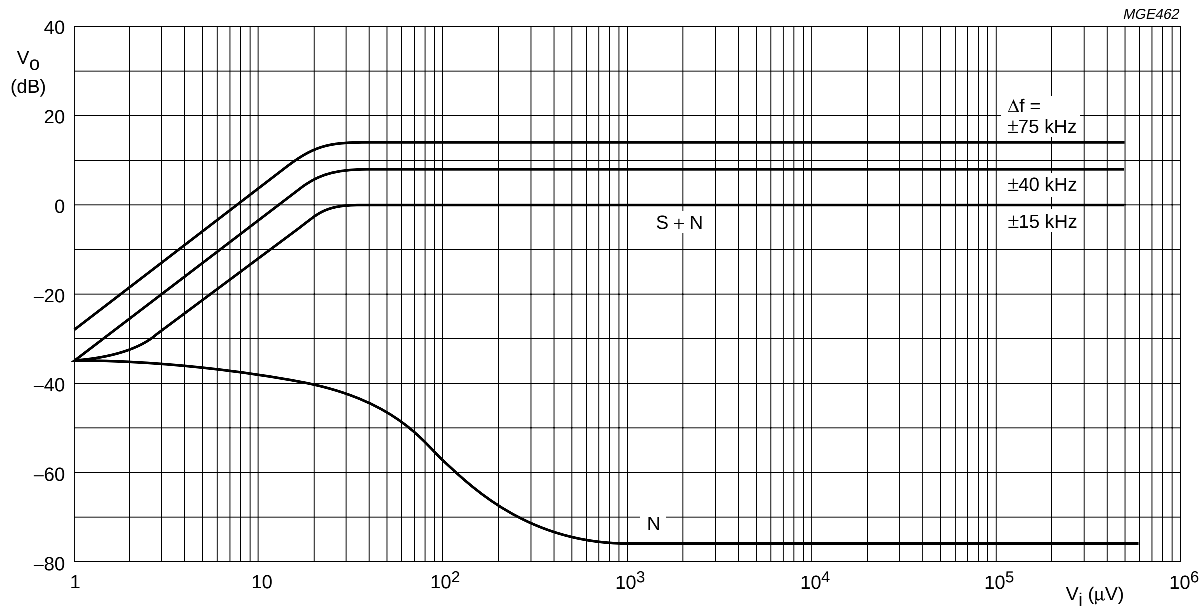


Fig.6 AF output voltage level as a function of IF input voltage; V_P = 15 V; f_m = 400 Hz; B = 250 Hz to 16 kHz; Q_L = 20; C_{8-9} = 6.8 nF.

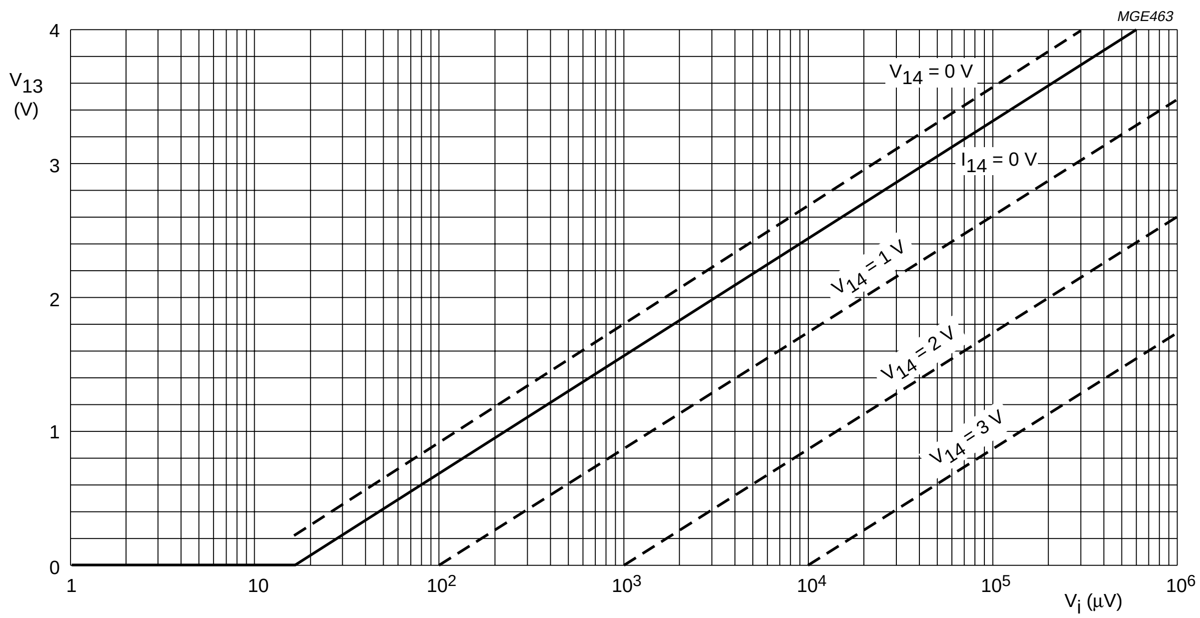


Fig.7 Voltage at field strength indicator output (proportional to V_{12}); R_{13} = 3.6 kΩ.

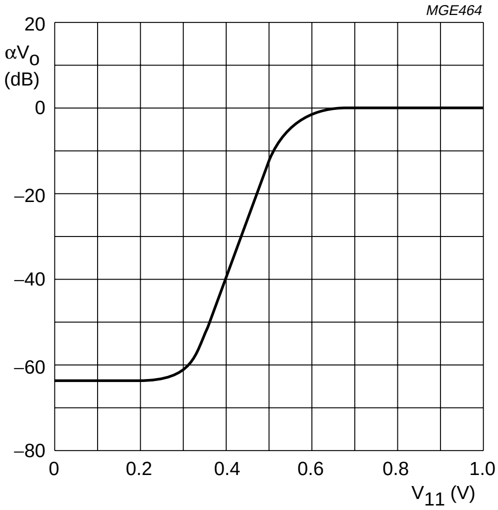


Fig.8 Attenuation of output voltage (αV_o) as a function of the muting control voltage V_{11}.

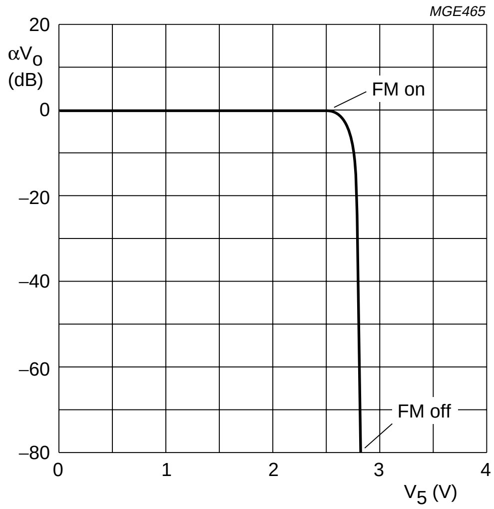
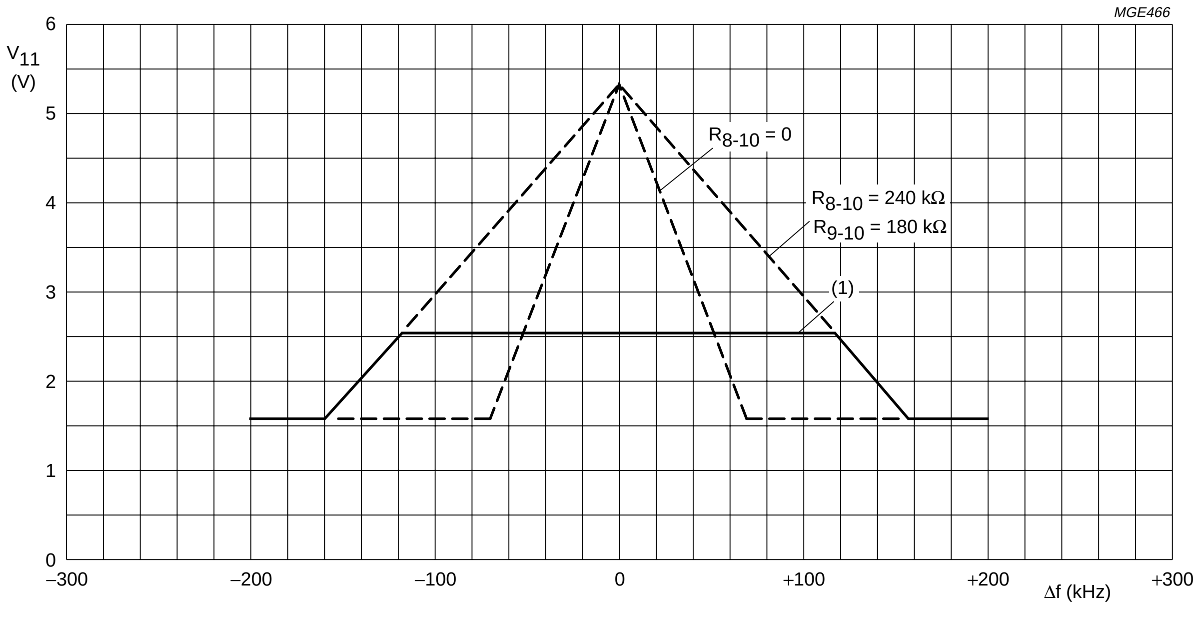
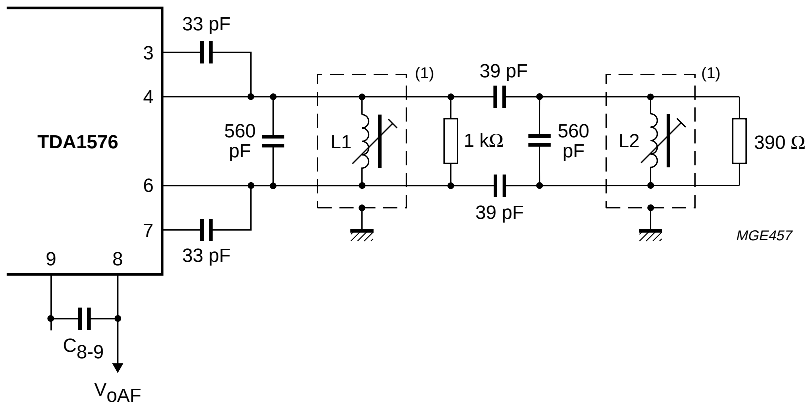


Fig.9 FM on/FM off standby switch; attenuation of output voltage (αV_o) as a function of control voltage V_5.



(1) Limited by external preset ($\alpha \times V_{12-18}$).

Fig.10 Detuning detector output voltage; V_P = 7.5 to 20 V; Q_L = 20.



Adjustment of the demodulator circuit is obtained with an IF signal which is higher than the 3 dB limiting level; L2 should be short-circuited or detuned; L1 should be adjusted to minimum d_2 distortion, and then L2 to minimum d_2 distortion.

(1) Coil data: L1 = L2 = 0.38 µH; Q_o = 70; coil former KAN (C).

Fig.11 An example of the TDA1576 when using a demodulator with two tuned circuits.

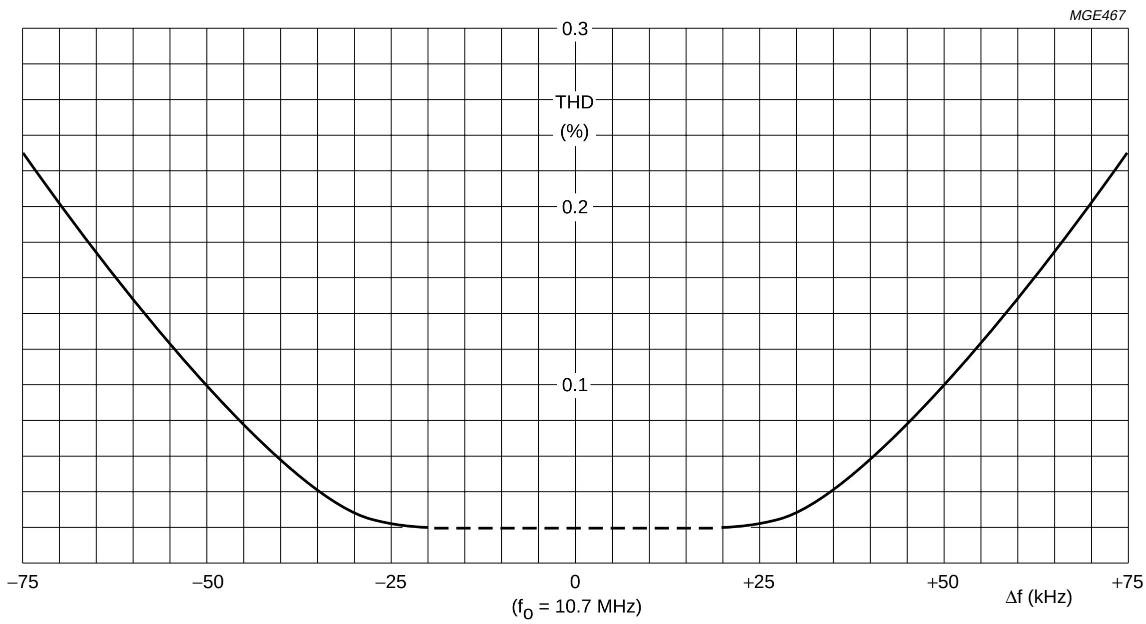
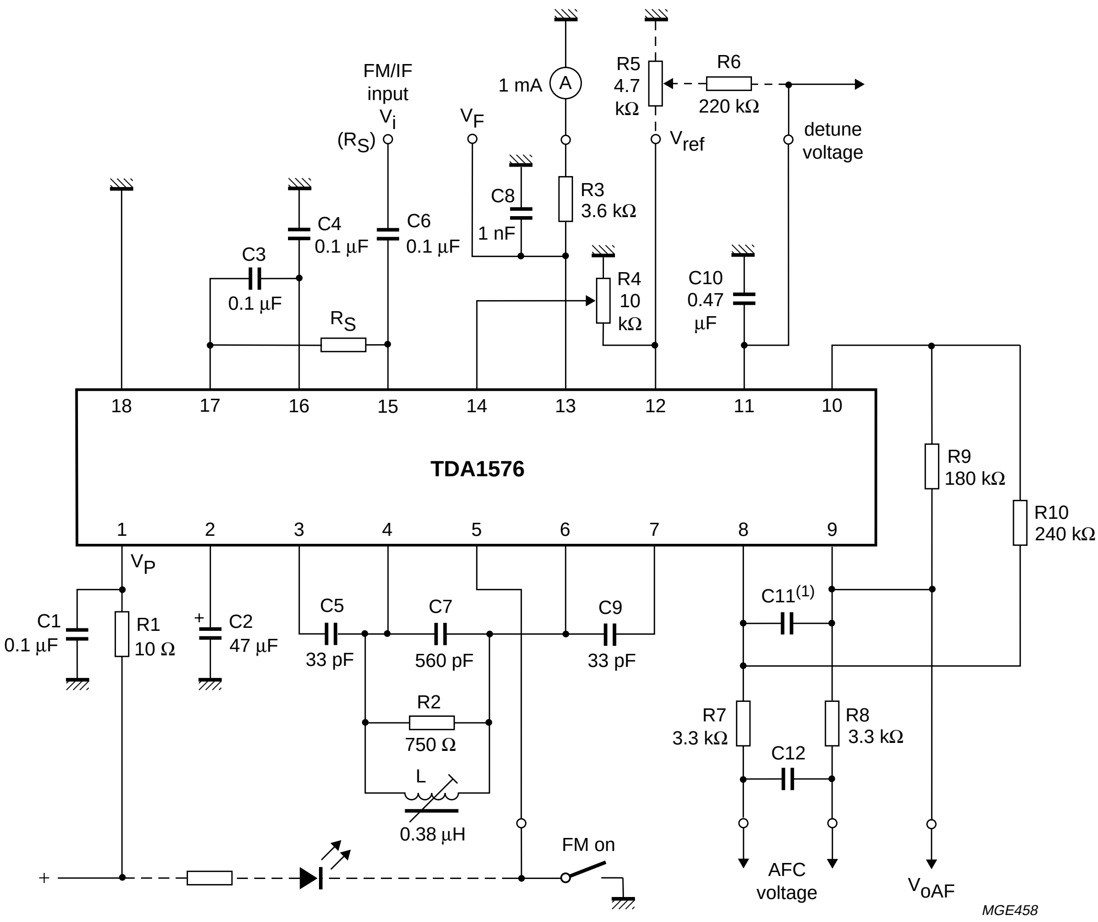


Fig.12 Total harmonic distortion as a function of detuning; f_m = 400 Hz; C_{8-9} = 6.8 nF; Δf = ±75 kHz; V_o = 330 mV for a frequency deviation Δf = ±75 kHz.

APPLICATION INFORMATION

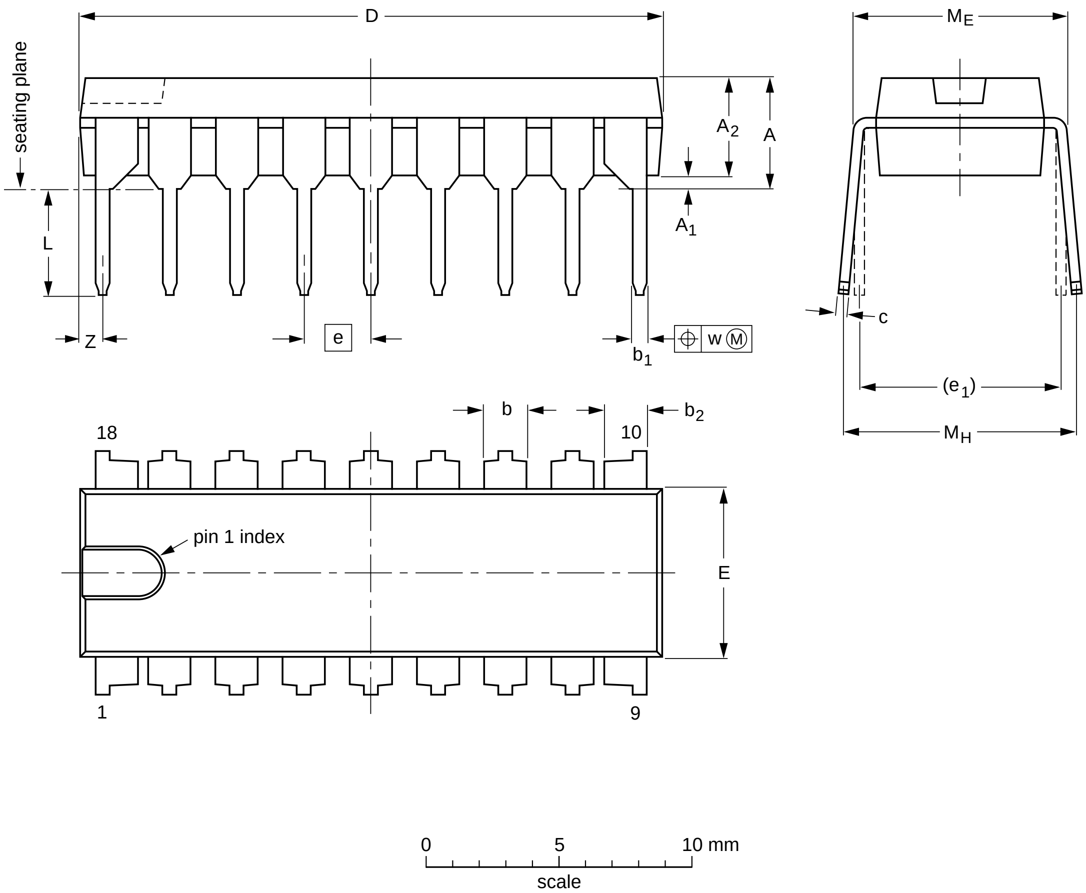


(1) For mono C11 = 6.8 nF; for stereo C11 = 56 pF.

Fig.13 Application diagram.

PACKAGE OUTLINE

DIP18: plastic dual in-line package; 18 leads (300 mil) **SOT102-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.7	0.51	3.7	1.40 1.14	0.53 0.38	1.40 1.14	0.32 0.23	21.8 21.4	6.48 6.20	2.54	7.62	3.9 3.4	8.25 7.80	9.5 8.3	0.254	0.85
inches	0.19	0.020	0.15	0.055 0.044	0.021 0.015	0.055 0.044	0.013 0.009	0.86 0.84	0.26 0.24	0.10	0.30	0.15 0.13	0.32 0.31	0.37 0.33	0.01	0.033

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT102-1						~~93-10-14~~ 95-01-23

SOLDERING

Introduction to soldering through-hole mount packages

This text gives a brief insight to wave, dip and manual soldering. A more in-depth account of soldering ICs can be found in our *"Data Handbook IC26; Integrated Circuit Packages"* (document order number 9398 652 90011).

Wave soldering is the preferred method for mounting of through-hole mount IC packages on a printed-circuit board.

Soldering by dipping or by solder wave

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joints for more than 5 seconds.

The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg(max)}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Manual soldering

Apply the soldering iron (24 V or less) to the lead(s) of the package, either below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

Suitability of through-hole mount IC packages for dipping and wave soldering methods

PACKAGE	SOLDERING METHOD	
	DIPPING	WAVE
DBS, DIP, HDIP, SDIP, SIL	suitable	suitable[(1)]

Note

1. For SDIP packages, the longitudinal axis must be parallel to the transport direction of the printed-circuit board.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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